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CSE211
Computer Organisation and Design

Q1:-In memory read the operation puts memory address on to a register known as :

a.PC

b.ALU

c. MAR

d. All of these

Q2:- In 3 state gate third position termed as high impedance state which acts as:

A-Open circuit

B- Close circuit

C- None of these

D- All of above

Q3. How is the effective address of base-register calculated?

a. By addition of index register contents to the partial address in instruction
b. By addition of implied register contents to the partial address in instruction
c. By addition of PC register contents to the complete address in instruction
d. By addition of implied register contents to the complete address in instruction

Q4:-Shift left is equal to:

a. multiply by two

b. add by two

c. divide by two

d. subtract by two

Q5. Which register holds the address for a stack whose value is supposed to be directed at the topmost position?

a. Stack Pointer
b. Stack Register
c. Both a & b
d. None of the above

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Question : When we use auto increment or auto decrements, which of the following is/are true?

1) In both, the address is used to retrieve the operand and then the address gets altered

2) In auto increment the operand is retrieved first and then the address altered

3) Both of them can be used on general purpose registers as well as memory locations

A-1,2
B-2,3
C-1
D-3

Q7:-In which of these addressing modes, a constant is specified in the instruction, after the opcode byte?

a) register instructions

b) register specific instructions

c) direct addressing

d) immediate mode

Q8:-The contents of the program counter is the _____ of the instruction to be run:

a. Data

b. Address

c. Counter

d. None of these

Q9:-The return address of the Sub-routine is pointed to by _____

a) IR

b) PC

c) MAR

d) Special memory registers

Q10:- In the case of, Zero-address instruction method the operands are stored in _____

a) Registers
b) Accumulators
c) Push down stack
d) Cache

Q11:- The addressing mode which makes use of in-direction pointers is _____

a) Indirect addressing mode
b) Index addressing mode
c) Relative addressing mode
d) Offset addressing mode

Q12:-The computer architecture aimed at reducing the time of execution of instructions is _____

a) CISC
b) RISC
c) ISA
d) ANNA

Q13:- The addressing mode, where you directly specify the operand value is _____

a) Immediate
b) Direct
c) Definite
d) Relative

Q14:-The circuit used to store one bit of data is known as

(A) Register

(B) Encoder

(C) Decoder

(D) Flip Flop

Q15:-The load instruction is mostly used to designate a transfer from memory to a processor register known as

(A) Accumulator
(B) Instruction Register
(C) Program counter
(D) Memory address Register

Q16:-Which are stages of instruction cycle:

a) Fetch
b) Decode
c) Execute
d) Derive effective address of the instruction
e) All of these

ANSWERS:—

Q1- C
Q2-A
Q3-A
Q4-A
Q5-A
Q6-B
Q7-D
Q8-B
Q9-B
Q10-C

Q11-A
Q12-B
Q13-A
Q14-D
Q15-A
Q16-E